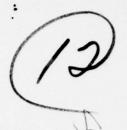
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PROCESS VARIABLE DEPENDENCE AND INTERRELATIONSHIP BETWEEN AVALANCHE INJECTED AND RADIATION INDUCED CARRIER TRAPPING IN THERMAL OXIDES

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Progress Report, No. 2,

1 July 1979 through 30 September 1979.

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Quarterly Status Report No. 2

Covering the Period 1 July 1979 through 30 September 1979

This is the second quarterly report on the ARPA sponsored project titled "PROCESS VARIABLE DEPENDENCE AND INTERRELATIONSHIP BETWEEN AVALANCHE INJECTED AND RADIATION INDUCED CARRIER TRAPPING IN THERMAL OXIDES." Progress to date includes the completion of the automated avalanche carrier injection and trapping system, the preparation of samples to study hole and electron trapping in dry as well as wet oxides, and the measurements of the effects of various process parameters on the trapping characteristics of thermal SiQ.

Experimental Procedure

The automated avalanche injection carrier trapping system is now complete. The system is capable of measuring flatband voltage changes as a result of the avalanche injection and trapping of both electrons or holes in thermal SiO₂ from p- and n-type silicon substrates, respectively.

The samples used in the experiment are n-type (111) silicon wafers, resistivity $0.2\text{-}0.3~\Omega\text{-cm}$, or p-type (111) wafers resistivity $0.4\text{-}0.7~\Omega\text{-cm}$. The wafers are oxidized in dry 0_2 or pyrogenic steam at 900°, 1000°, and 1100°C to an oxide thickness of approximately 800 Å. Following oxidation the wafers are cooled in the oxidizing ambient [02 fast pull (<3 sec), 02 slow pull (10 min), H20 pull (<30 sec)] or in an inert ambient following a 10 min anneal [N2 slow pull (2 min), Ar slow pull (2 min)]. The oxide is then removed from the back of the wafers and Al-Cu-Si deposited by cold flash on both sides of the wafers. Metal dots (30 mils in diameter) are defined by photolithography and one half of each wafer is annealed in N2 at 400°C for 10 minutes while the other half receives a post-metallization anneal in a 10% H2 in N2 ambient at 400°C for 10 min.

Tables I through IV identify the various runs by number and process sequence. The tables also show the number of fixed oxide charges (N_f) and the interface state density at midgap (D_{it}).

TABLE I

Values of Fixed Oxide Charge $(Q_{\mathbf{f}})$ and Interface State Density $(\mathbf{D}_{\mathbf{i}\mathbf{t}})$ For N-Type (111) Silicon Wafers Oxidized in Steam

	Oxidation Temp	0x/ Annea1	Ox/ Anneal/Cool		Oxide Thickness		Qf/q (1011/cm ²) [†]	Midgap Dit [†] (10 ¹¹ /cm ² -eV	Dit [†] m ² -eV)
Run No.	(0°)	Ambient	Time*(min)	Condition**	(m ^{rl})	N ₂ Anneal	H ₂ Anneal	N ₂ Anneal	H ₂ Anneal
TR-1	006	02/-	300/0/0		0.079	•	∞ c		
TR-3	:	02/N2	-	N2 SP	0.079	2.96	2.35	29.0	0.54
TR-4	:		300/10/2		0.081	•	2		
JTR-5	1000	-/20	84/0/0						6
TR-6	:	02/-	0/			•			4
TR-7	:	02/N2	84/10/2	N ₂ SP	0.084	2.13	1.70	0.72	0.40
TR-8	:	02/AF	/10			•	•		7
TR-9	1100	-/20	28/0/0	02 FP		-	3.45	1.62	-
TR-10	:		28/0/10	02 SP	0.088	7.16	8.00	1.67	2.21
TR-11	:	02/N2	28/10/2		•	2		0.41	-
TR-12	:	02/Ar	/10/		•	1	•	0.34	

time	
or Ar/Pull	
or	
N,	0,
in	in
time	sec)
oxidation time/anneal	** = 02 FP = fast pull (<3 sec) in 07
11	11
*	*

02 SP = slow pull (10 min) in 02 N2 SP or Ar SP = slow pull (2 min) in N2 or Ar = average of three or more capacitors

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TABLE II

Values of Fixed Oxide Charge $(Q_{\mathbf{f}})$ and Interface State Density $(\mathbf{D}_{\mathbf{i}\mathbf{t}})$ For P-Type (111) Silicon Wafers Oxidized in Dry Oxygen

	Oxidation	0x/ Anneal	0x/ Anneal/Cool	C001	Oxide Thickness	Q _f /q (10	$Q_{\rm f}/q \ (10^{11}/{\rm cm}^2)^{+}$	Midga (10 ¹¹ /c	Midgap Ditt
Run No.	(°C)	Ambient		Condition**	(h m)	N2 Anneal	H ₂ Anneal	N ₂ Anneal	H ₂ Anneal
TR-21	0	-/20	300/0/0		0.081			0.88	0.85
TR-22	=	02/-	300/0/10		0.082			1.01	1.00
TR-23	:	02/N2	300/10/2	N ₂ SP	0.080	3.24	2.94	0.62	0.56
TR-24	:	02/Ar	300/10/2		0.081	•	•	0.52	0.59
TR-17	1000	02/-	84/0/0		0.080		4.84	0.89	0.83
TR-18	=	02/-	84/0/10	0 ₂ SP	0.086	6.65	7.08	1,61	0.94
TR-19	:	02/N2	84/10/2		0.081	•	.2.34	0.40	0.37
TR-20	:	02/Ar	84/10/2		0.080	•	2.60	0.37	0.45
TR-13	1100	-//0	28/0/0				3.45	0.62	0.63
TR-14	:	02/-	28/0/10	02 SP	0.089	8.04	7.70	1.04	1.03
TR-15	:	02/N2	28/10/2		•		2.13	0.37	0.35
TR-16	:	02/Ar	28/10/2		•	•	1.50	0.36	0.35
* oxid	oxidation time/anneal time	anneal t	in N2 or	Ar/Pull time				RRR 10/9/79	

oxidation time/anneal time in N₂ or Ar/Pull time 0₂ FP = fast pull (<3 sec) in 0₂ 0₂ SP = slow pull (10 min) in 0₂ N₂ SP or Ar SP = slow pull (2 min) in N₂ or Ar average of three or more capacitors

TABLE II

Values of Fixed Oxide Charge (Q_f) and Interface State Density $(D_{1\,t})$ For P-Type (111) Silicon Wafers Oxidized in Dry Oxygen

		Oxidation	/x0	/x0		0xide	017 0/ 0	2 /2 (1011 /2-2)+	Midge	Midgap Ditt
		Temp	Annea1	Anneal/Cool	Coo1	Thickness	or) h/Jh	/cm-)T		(10 ¹¹ /cm ² -eV)
Run	No.	(ac)	Ambient	Time*(min)	Condition**	(m n)	N2 Anneal	H ₂ Anneal	N ₂ Anneal	H ₂ Anneal
TR-	21	006	-/20	300/0/0		0.081	5.05	5.20	0.88	0.85
TR-22	.22	:	02/-	300/0/10	02 FP	0.082	6.43	6.51	1.01	1.00
TR-	.23	:	02/N2	300/10/2		0.080	3.24	2.94	0.62	0.56
TR-	.24	:	02/Ar	300/10/2		0.081	3.31	3.32	0.52	0.59
TR-	17	1000	02/-	84/0/0		0.080		4.84	0.89	0.83
TR-1	-18	=	02/-	84/0/10	0 ₂ SP	0.086	6.65	7.08	1.61	0.94
TR-1	.19	:	02/N2	84/10/2		0.081	•	.2.34	0.40	0.37
TR-20	-20	=	02/Ar	84/10/2		0.080	•	2.60	0.37	0.45
TR-	13	1100	-/'0	28/0/0		0.079	3,53	3.45	0.62	0.63
TR-14	.14	=	02/-	28/0/10	02 SP	0.089	8.04	7.70	1.04	1.03
TR-	.15	=	02/N2	28/10/2		080.0	1.65	2.13	0.37	0.35
TR-	.16	:	02/Ar	28/10/2		0.080	1.44	1.50	0.36	0.35
**	oxida	oxidation time/anneal time	unneal time	in N2 o	r Ar/Pull time				RRR 10/9/79	

** O2 FP = fast pull (<3 sec) in O2
O2 SP = slow pull (10 min) in O2
N2 SP or Ar SP = slow pull (2 min) in N2 or Ar
+ average of three or more capacitors

Table III

Values of Fixed Oxide Charge (Q_f) and Interface State Density (D_{it}) For N-Type (111) Silicon Wafers Oxidized in Steam

	Oxidation Temp.	Anneal		C001	Oxide Thickness	Q _f /q (10	Q _f /q (10 ¹¹ /cm ²)*	Midgap D_{1t}^* (10 ¹¹ /cm ² -eV)	D1t* 12-eV)
Run No.		Ambient	Time (min)	Condition	(mn)	N2 Anneal	H ₂ Anneal	N2 Anneal H2 Annea	H ₂ Annea
TR-25	006	-/0211	20/0/0		0.082	4.10	4.03	0.90	1.17
TR-26	=	H20/N2	20/10/2	N ₂ SP	0.083	2.43	2.38	0.43	0.45
TR-27	:	H20/Ar	20/10/2		0.083	2.80	2.40	0.34	0.47
TR-28	1000	H ₂ 0/-	2/0/0		0.080	3.50	3.63	0.56	0.62
TR-29	:	1120/N2	5/10/2	N ₂ SP	0.082	2.17	1.71	0.32	0.31
TR-30	=		5/10/2		0.081	2.67	2.27	0.23	0.40
TR-31	1100	H ₂ 0/-	1.75/0/0		0.087	3.81	. 4.12	0.78	0.84
TR-32	:	1120/N2	1.75/10/2	N ₂ SP	0.087	1.80	1.62	0.26	0.24
TR-33	:	1120/Ar	1.75/10/2		0.087	1.78	1.76	0.40	0.30
-		The other parameters and the second							

* Average of three or more capacitors

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Table IV

Values of Fixed Oxide Charge (Q_f) and Interface State Density (D_{it}) For P-Type (111) Silicon Wafers Oxidized in Steam

	Oxidation Temp.	0x/ Anneal	0x/ Anneal/Cool	C001	Oxide Thickness	Qf/q (10 ¹¹ /cm ²)*	.1/cm ²)*	Midgap Dit* (1011/cm ² -eV)	Midgap Dit* (011/cm ² -eV)
Run No.	(2,)	Ambient	Ambient Time (min)	Condition	(mm)	N ₂ Anneal	H ₂ Anneal	N ₂ Anneal H ₂ Annea	H ₂ Annea
TR-40 TR-41 TR-42	.006	H ₂ 0/- H ₂ 0/N ₂ H ₂ 0/Ar	1.75/0/0 1.75/10/2 1.75/10/2	H ₂ O FP N ₂ SP Ar SP	0.080 0.080 0.082				
TR-37 TR-38 TR-39	1000	H2O/- H2O/N2 H2O/Ar	5/0/0 5/10/2 5/10/2	H20 FP N2 SP Ar SP	0.077 0.080 0.077				
TR-34 TR-35 TR-36	1100	H ₂ 0/- H ₂ 0/N ₂ H ₂ 0/Ar	20/0/0 20/10/2 20/10/2	H ₂ O FP N ₂ SP Ar SP	0.078 0.088 0.081				

RRR 10/5/79

*Average of three or more capacitors

Results and Discussion

Characterization of fixed oxide charge density and interface trapped charge density (at midgap) has been carried out for n- and p-type samples prior to the avalanche injection and trapping experiments. Results to date are included in Tables I through III. Some points of interest in the process dependence of the interface charges are:

- (a) lowest densities of charges are obtained for samples annealed in situ following oxidation either in nitrogen or argon,
- (b) lower charge densities are obtained for samples oxidized at higher temperatures.

These results conform with our previous observations and are typical of the process sequences outlined in the tables.

1. Hole Trapping in Dry 02 Oxides

The results obtained from the hole trapping experiments are summarized in Fig. 1. Flatband voltage shifts are shown versus oxidation temperature for samples oxidized in dry O_2 with various cooling conditions, and given a post-metallization anneal in a 10% H₂ in N₂ ambient at 400%C for 10 min. A constant average current of 4.5×10^{-8} A/cm² was maintained during injection and values of flatband voltage shift shown are for injection times of 2000 sec.

Post-oxidation in situ annealing is observed to increase hole trapping considerably at higher temperatures particularly 1100°C. A slight increase is also noted for oxygen pulled samples with 900°C O₂ cooled samples yielding the least hole trapping.

Considering a model where the probability of trapping is proportional to the number of unfilled traps (1) the shift in flatband voltage is given by

$$\Delta V_{FB} = \frac{qN_{eff}}{C_{ox}} \left(1 - e^{-\sigma Jt/q} \right)$$

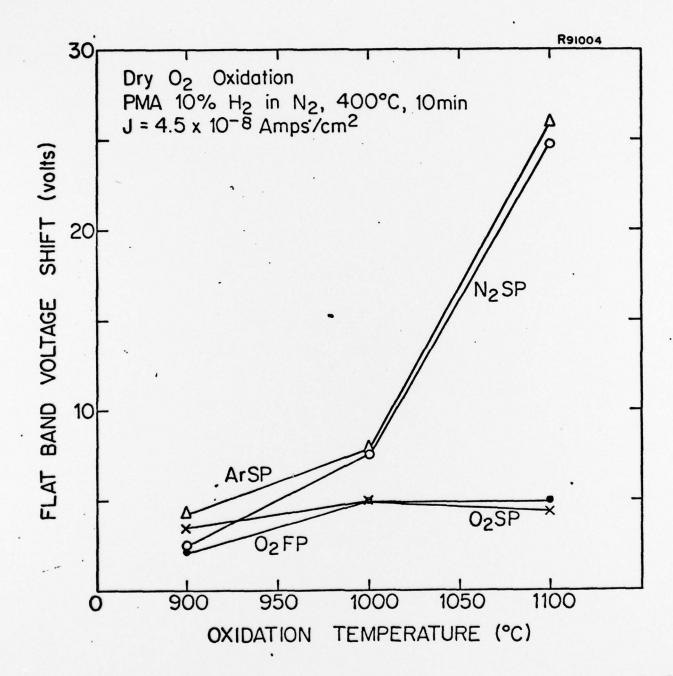


Fig. 1. Flatband voltage shift versus oxidation temperature for hole trapping by avalanche injection from n-type (111) substrates. Samples were oxidized in dry O2 and received a post metallization anneal at 400°C in a 10% H2 in N2 ambient for 10 minutes. Flatband voltage shifts are for 2000 sec injection time.

taking the derivative with respect to time

$$\frac{d}{dt} \Delta V_{FB} = \frac{d}{dt} V_{FB} = \frac{qN_{eff}}{C_{ox}} \left(\frac{\sigma J}{q}\right) e^{-\sigma Jt/q}$$

and

$$\ln \left[\frac{d}{dt} \ (V_{FB})\right] = \ln \ \frac{qN_{\mbox{\footnotesize eff}}}{C_{\mbox{\footnotesize ox}}} \ \left(\frac{\sigma J}{q}\right) - \frac{\sigma J}{q} \ t$$

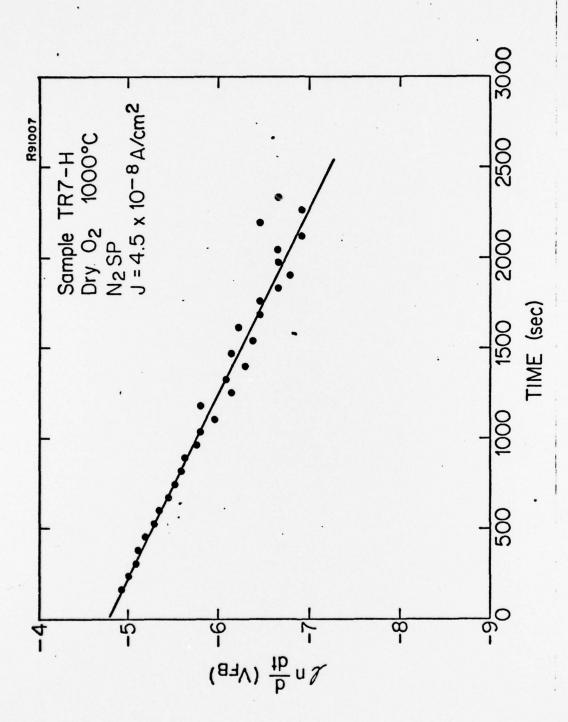
A plot of the ln $\left[\frac{d}{dt} \, V_{FB}\right]$ versus injection time t will yield a straight line in the case of a single trap, the slope of which allows the computation of the capture cross section and the intercept gives information on the effective trap density. Figure 2 shows the results obtained from sample TR7-H, which was oxidized in dry 0_2 , at $1000\,^{\circ}$ C, annealed in situ in nitrogen, and cooled in N_2 . A single trap seems dominant in this case of cross section $3.5 \times 10^{-15} \, \mathrm{cm}^2$ with an effective trap density of about $2 \times 10^{12}/\mathrm{cm}^2$.

Variations in low temperature post-metallization annealing was investigated by using two different annealing processes "400°C, 10 min, 10% H₂ in N₂" and "400°C, 10 min, N₂" indicate no substantial detrimental effects from the addition of the 10% hydrogen in the ambient.

2. Electron Trapping in Dry 0, Oxides

Measurements have not beem completed to date on all samples in this group. Preliminary results indicate smaller trapping cross sections for electrons as expected. Postoxidation anneals in nitrogen or argon at higher temperatures do not have the drastic effects observed in hole trapping.

Interface traps generated by the avalanche injection are also being monitored for selected samples in this set. Figure 3 shows the increase in interface traps at midgap as a function of time for a sample oxidized in dry 0, at 900°C and cooled slowly in the oxidizing ambient. A rapid build up of states is observed at times less than 1000 sec, followed by a relatively constant generation rate and a slight decrease in the generation rate at times greater than 3500 sec. More



An d/dt (VFB) versus time for samples oxidized in dry 02 at 1000°C. The sample received an in situ anneal in nitrogen for 10 min and was cooled in N2. The post metallization anneal treatment was: 400°C, 10% H2 in N2, 10 min. Fig. 2.

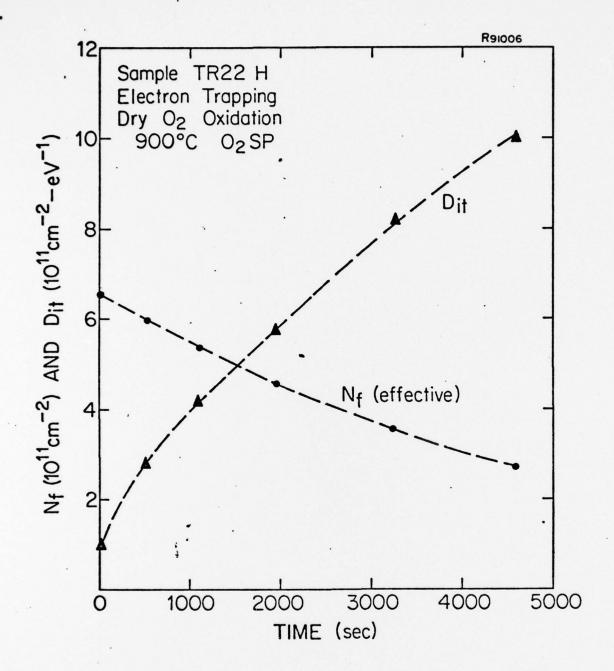


Fig. 3. Effective fixed oxide charge density Nf and interface trapped charge density Dit versus injection time.

measurements are being carried out in order to characterize the behavior of interface traps during avalanche injection and their dependence on process variables.

Electron Trapping in Pyrogenic Steam Oxides

Measurements have been started on the characterization of the process dependence of avalanche carrier injection and trapping in pyrogenic steam oxides. Results of electron trapping are shown in Fig. 4 for samples oxidized at 900°C. Substantial trapping was noted for all samples particularly those cooled in steam. These steam cooled samples showed a very rapid increase in flatband voltage followed by a decrease, and a subsequent slight increase at large injection times. This decrease in flatband voltage shift has been observed previously (2) and is possibly related to a rapid increase in interface traps. The details of interface trapped charge behavior will be investigated in the coming months in order to verify this conclusion.

The program schedule is enclosed and the program is essentially on schedule. Some measurements for electron trapping in dry 0, are not yet completed, but electron trapping in steam oxides are ahead of schedule. Results of radiation induced carrier trapping to be carried out at the Naval Research Laboratories are not available to date. Comparison of avalanche induced and radiation induced trapping should be quite interesting.

References

- 1. T. H. Ning and H. N. Yu, J. Appl. Phys., 45, 5373 (1974).
- 2. R. A. Gdula, J. Electrochem. Soc., 123, 42 (1976).

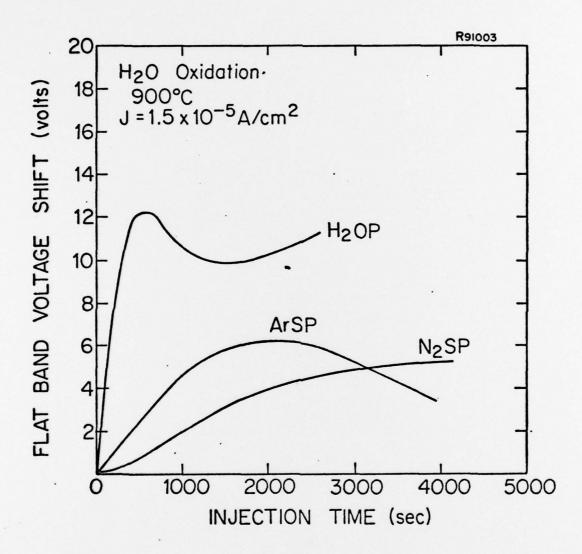


Fig. 4. Flatband voltage shift versus injection time for wafers oxidized in pyrogenic steam at 900°C for various cooling procedures. Post oxidation anneal: 400°C, 10% H₂ in N₂, 10 min.

